REMARKS

Claim 1 has been amended to incorporate the allowable subject matter of claim 2 and claim 2 has been cancelled without prejudice or disclaimer. Claims 1 and 3-15 are pending and under consideration. No new matter is presented in this Amendment. Claims 1 and 14 are the independent claims.

DOUBLE PATENTING:

Claims 14-15 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-2 of Copending application 10/828,327.

Since claims 14-15 of the instant application have not yet been indicated as allowable, it is believed that any submission of a Terminal Disclaimer or arguments as to the non-obvious nature of the claims would be premature.

As such, it is respectfully requested that Applicant be allowed to address any provisional obviousness-type double patenting issues remaining once the rejections of claims 14-15 under 35 U.S.C. §§102 and 103 are resolved.

REJECTIONS UNDER 35 U.S.C. §102:

Claim 1 is rejected under 35 U.S.C. §102(b) as being anticipated by Matsui (U.S. Patent No. 5,661,707).

Applicant notes that claim 1 has been amended to incorporate the allowable subject matter of claim 2.

Accordingly, Applicant respectfully asserts that claim 1 is in condition for allowance and requests that the rejection of claim 1 under 35 U.S.C. § 102(b) be withdrawn.

Claim 14 is rejected under 35 U.S.C. §102(e) as being anticipated by Ichikawa (U.S. Patent No. 5,901,159).

Applicant respectfully traverses this rejection for at least the following reason.

Independent claim 14 recites a data scrambling method comprising: scrambling data having structure of 2 KB for a sector or a data frame and 64 KB for an error correction code (ECC) block based on random data in a cycle of 32 KB.

The Office Action relies on Ichikawa for such teachings and in particular cites column 14, lines 50-67 and column 15, lines 1-30.

A review of Ichikawa and of the cited columns indicates that Ichikawa discloses a digital signal decoder which decodes coded data, for example, a coded digital video signal having error-correcting data such as C1/C2 convolutional Reed-Solomon type data added thereto. The decoder stores in a memory the coded data, detects correctable errors in the stored coded data, ascertains positions of the detected errors in the coded data, and supplies error correction patterns that correspond to those errors. A second memory stores the ascertained positions of the errors as well as the error correction patterns, and coded data that correspond to the positions of the errors are read from the first memory and decoded by using the error correction patterns stored in the second memory so as to produce corrected decoded data (abstract).

Ichikawa further discloses that the data is recorded in units of 32Kb data clusters (Fig. 22 and column 13, lines 21-24). Ichikawa also discloses the data structure of a sector and how the main data of the sector shown in FIG. 25 is scrambled by exclusively logically adding together the main data with scramble data generated using as the initial value a value specified by the lower 4 to 7 bits of the physical sector address (column 15, lines 1-5).

Accordingly, although Ichikawa discloses a data scrambling method, as well as a data structure and a data block, such as an ECC, Ichikawa makes no reference or suggestion to the data scrambling method comprising: scrambling data having a structure of 2 KB for a sector or a data frame and 64 KB for an error correction code (ECC) block based on random data in a cycle of 32 KB.

As a matter of fact, nowhere in the specification does Ichikawa disclose 64KB for an ECC block.

Accordingly, Applicant respectfully asserts that the rejection of claim 14 under 35 U.S.C. § 102(b) should be withdrawn because Ichikawa fails to teach or suggest each feature of independent claim 14.

REJECTIONS UNDER 35 U.S.C. §103:

Claim 15 is rejected under 35 U.S.C. §103(a) as being unpatentable over Ichikawa (U.S. Patent No. 5,901,159), and further in view of Unno (U.S. Patent No. 6,577,647).

Applicant respectfully traverses this rejection for at least the following reason.

Initially it is noted that claim 15 depends from independent claim 14, and as noted above, Ichikawa fails to teach or suggest the novel features of independent claim 14.

Furthermore, it is noted that Unno is relied upon for a teaching of features other than those recited in independent claim 14. Accordingly, Unno fails to cure the deficiencies of Ichikawa.

Finally, Applicant notes that Unno is relied upon for a teaching of shifting left a 15-bit serial register r_0 through r_{14} for generating random data synchronously with a clock input for scrambling; outputting an exclusive OR value exclusive-ORing output from the higher-most register r_{14} and output from the lower register r_{10} to the lower-most register r_0, outputting the result of exclusive-ORing 1-byte input data D_0 through D_7 and each of the 8 outputs of the lower registers r_0 through r_7 after left-shifting the 15 bit register r_0 through r_{14} 8 times.

However, a careful review of Unno and the cited passages reveals that Unno does not in fact teach the novel features of claim 15 and thus Applicant respectfully traverses this rejection for at least the following reasons.

Unno discloses a synchronization system and a synchronization method for strict commercial time synchronization by advancing the timing of generation of a PN (Pseudo-random Noise) signal in an upstream station by a transmission line delay.

Unno further discloses in FIG. 4 a block diagram illustrating the configuration of each of the PN generators. Each of the PN generators consists of shift registers of 15 stages 101 to 115 and exclusive-OR circuits 201 to 205. The period of a PN signal generated by each of these PN generators is $(2^{15}-1)$ times the unit bit duration thereof. That is, the period of an output sequence of each of these PN generators is 32767 $(=2^{15}-1)$ bits. Thus, each of these PN generators repeatedly outputs a pseudo-random code of the same pattern every period of 32767 bits (column 6, lines 1-8).

Accordingly, although Unno discloses a generator including shift registers and exclusive-OR circuits, Unno des not teach or suggest the scrambling process recited in claim 15.

Therefore, Applicant respectfully asserts that dependent claim 15 is allowable at least because of its dependency from claim 14, and because it includes additional features which are not taught or suggested by the prior art. Therefore, it is respectfully submitted that claim 15 also distinguishes over the prior art.

ALLOWABLE SUBJECT MATTER:

Claims 2-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

CONCLUSION:

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 503333.

Respectfully submitted,

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